Chip Design of White LED Driver

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Abstract

The portable electronic products are widely used in daily life. Because most of these products need screen or backlight, the white LED is popularly applied to these products. In many applications, we need an IC driver to supply the necessary power to drive the White LEDs. There are two kinds of drivers, parallel type and series type, each of them has its own advantages and disadvantages. The parallel one can be fabricated with standard CMOS process instead of using the wing high voltage CMOS process.

In this paper, we will present the process of implementing a white LED driver chip. It is using Taiwan Semiconductor TSMC's Manufacture Inc. 0.35 um 2P4M process. The circuit designed with the described process can be operated at 3.2–5.5 V input voltage to generate 4.7–5.2 V output voltage. Maximum output current can be running up to 100 mA. This driver IC is implemented with capacitors instead of inductors to avoid possible electromagnetism interference.

The proposed circuit consists of voltage reference circuit, oscillator circuit and charge pump circuit. The circuit design, the theoretical analysis of the circuit, circuit simulation results and measured results are all discussed this paper.

The proposed driver can be applied in the white light LED driver, LED Brightness Controller, Li-Ion Battery recharge system, or a voltage supplier to supply 5 V voltage to PCMCIA.

***Key Words*:** White LED Driver, DC-DC Converter

1. Introduction

Due to the rapid development of electronic products, the portable electronic products have been widely used in the world. The electronic circuit is included in many digital products like cell phone or Personal Digital Assistant (PDA) and so on. Most of these products need to use screen or LED lamp for their display. In general, the backlight of LCD monitor is illuminated by Cold Cathode Fluorescent Lamps (CCFL), but the material used, mercury (Hg), is not good to our environment. Therefore many companies are developing White LED for the backlight. This White LED can be found in cell phone keyboard, camera phones, headlight and display board of car and daylight lamp. However, in these White LED products they need to increase the source supply voltage so as to get the best light efficiency. Currently, regular White LED driver works with the architectures of either series or parallel LEDs, each architecture has its own distinct advantages.

The circuits shown in Figures 1 and 2 are the two functional block diagrams of a regular White LED driver. The circuit shown in Figure 1 is the parallel architecture with charge-pump driver [1]. It can supply 100 mA output current or it can provide the required current sources for five parallel LEDs. The series architecture is shown in Figure 2 [2], its input supply voltage varies from 2.7 V to 4.7 V while its output voltage is 30 V. It can

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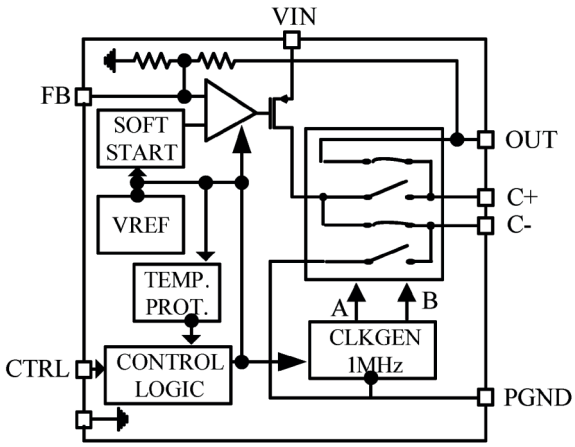

Figure 1. The parallel architecture of regular LED driver IC.

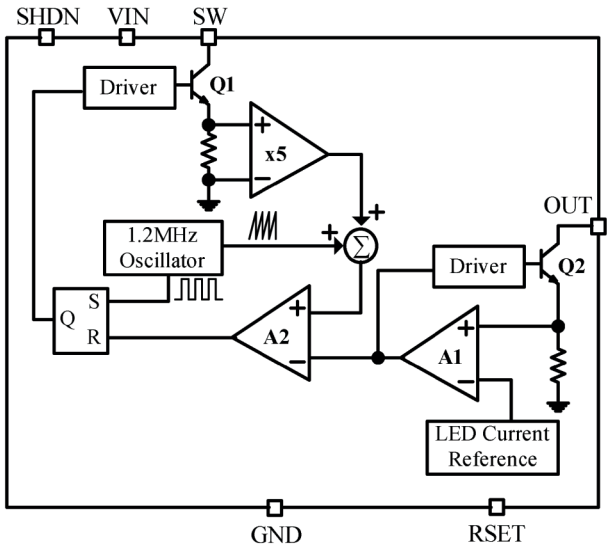

Figure 2. The serial architecture of regular LED driver IC.

drive five serial LEDs.

All portable electronic products need backlight in their display, and it also requires low power consumption in the light sources. It has advantages of low power consumption and low supply voltage in White LEDs. Therefore, White LED is a good candidate for light source. The supply voltage of Li-ion battery is from 2.7 V to 4.7 V. In order to extend the standby and usage times, we boost the input voltage in the White LED driver to 5 V.

2. Circuit Design

2.1 Bandgap Reference Circuit

A bandgap reference circuit to generate an output voltage that is independent of the supply voltage and temperature [3,4] will be discussed in this section. The bandgap reference circuit, as shown in Figure 3, can generate an output voltage with temperature coefficient of 10 ppm/°C within 0 to 70 °C range. The VBE is the junction voltage of the forward-biased diode with approximately -2.2 mV/°C temperature coefficient. The thermal voltage V_t (= kT/q), which is proportional to absolute temperature (PTAT), has a +85 uV/°C temperature coefficient at room temperature. The bandgap voltage V_{REF} can be calculated as [3],

$$V_{REF} = V_{BE} + KV_t \tag{1}$$

A conventional CMOS bandgap circuit with n-well process is shown in Figure 4 [4]. It includes in the circuit the input voltage offset of the op amp. The transistors Q_1 and Q_2 are assumed to have emitter-base areas of A_{E1} and A_{E2}, respectively. If the offset voltage V_{os} is assumed to have zero value, the voltage across R_1 is given by [3]

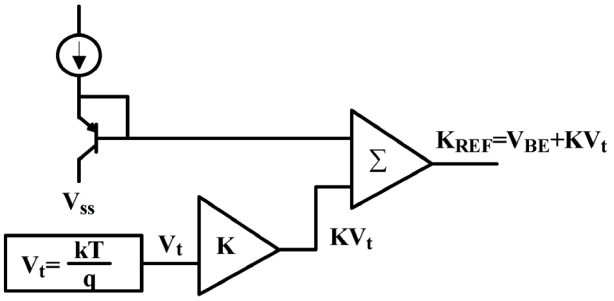

Figure 3. The operation of the bandgap circuit.

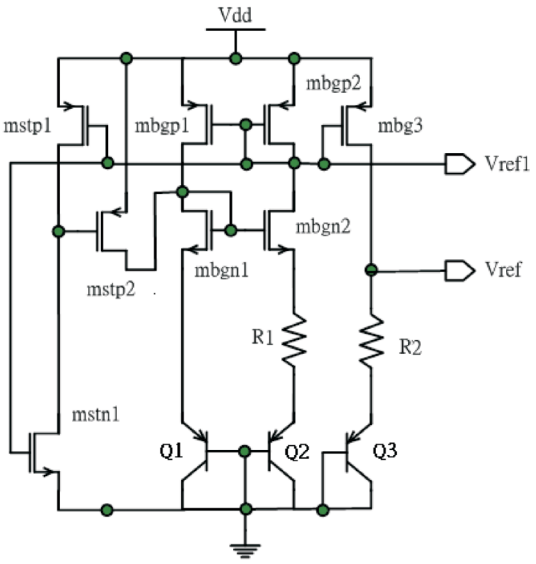

Figure 4. A PTAT bandgap circuit.

$$V_{R1} = V_{EB2} - V_{EB1} = V_t \ln(\frac{J_2}{Js2}) - V_t \ln(\frac{J_1}{Js2}) = V_t \ln(\frac{I_2 A_{E1}}{I_1 A_{E2}}) \quad (2)$$

If the op amp is connected with negative feedback then it has the relation [3],

$$I_1 R_2 = I_2 R_1 \quad (3)$$

As shown in Figure 4, the output voltage of the circuit can be expressed as

$$V_{ref} = V_{EB2} + I_2 R_3 = V_{BE2} + V_{R1}\left(\frac{R_2}{R_1}\right) \quad (4)$$

Substitute Eq. (2) into Eqs. (3) and (4), we have

$$V_{ref} = V_{EB2} + \left(\frac{R_2}{R_1}\right) V_e \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\right) \quad (5)$$

Comparing Eqns. (1) and (5), we get

$$K = \left(\frac{R_2}{R_1}\right) \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\right) \quad (6)$$

Thus, the constant K is proportioned to the resistor value and the bipolar area. We then consider the effect of the input-offset voltage on the output voltage. Eq. (1) can be rearranged as

$$V_{ref} = V_{EB2} - \left(1 - \frac{R_2}{R_1}\right) V_{os} + \left(\frac{R_2}{R_1}\right) V_e \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\left(1 - \frac{V_{os}}{I_1 R_2}\right)\right) \quad (7)$$

From Eq. (7), the variation in the output voltage due to the input offset voltage is small and it is independent of temperature.

The PTAT current generator has structure as shown in Figure 4 [3]. Its output voltage has the form as,

$$V_{ref} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n \quad (8)$$

In Eq. (7), it is assumed that all PMOS in the circuit are of the same size, this indicates that only V_{BE3} and Q_3 but no temperature will have effects on the reference voltage. If PMOS's are not matching each other, then it will introduce certain deviation in the output voltage.

The bandgap circuit, as shown in Figure 4, is selected in our design. In order to avoid bandgap circuit stalling at zero current state, a start-up circuit is employed. The start-up circuit consists of three MOSFETs denote as mstp1, mstp2 and mstn1. Devices mbgp1, mbgp2, mbgp3, mbgp4 and rvref1 in the circuit are employed to generate constant current. The current in the circuit is kept constant even if has variation in the supply voltage.

2.2 Design of Clock Generator Circuit

There are many kinds of oscillator circuits. One of the oscillator circuit is shown in Figure 5 [5]. Because we only employ ring oscillator circuit, we will discuss in detail of the ring oscillator circuit.

The ring oscillator circuit is popularly used in digital voltage control oscillator. [6] As shown in Figure 6 is a five-stage ring oscillator circuit with inverters. The inverter is used to invert the signal with 180 degree conversion, its output then inputs to the next stage. The last stage signal is feedback to the first stage input to close the loop. The loop can be designed to oscillate when an odd number of stages are implemented in the loop. The frequency of the ring oscillator is [6]

$$f_{osc} = \frac{1}{n(t_{PHL} + t_{PLH})} \quad (9)$$

Where, t_{PHL} is the delay time of inverter so as to raise the output signal while t_{PLH} is the delay time of the inverter that will lower the output signal. Assume all in-

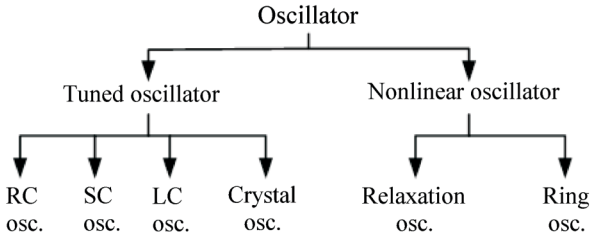

Figure 5. The classification of oscillator circuits.

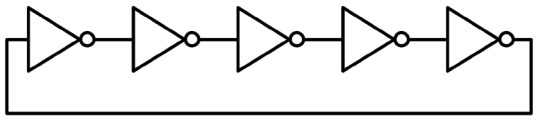

Figure 6. A five stage ring oscillator.

verters have the same characteristics and n is the number of inverters.

In order to find the optimum size of MOS in the design, we need to consider the incurring of the parasitic capacitance and parasitic resistance due to the introduce of the inverters. The total capacitance of the inverter is shown in Eq. (10)

$$C_{tot} = \underbrace{2C_{ox}}_{C_{out}} + \underbrace{3C_{ox}}_{C_{in}} = 5C_{ox} \tag{10}$$

The resistance of MOS is

$$R = \frac{V_{DD}}{\frac{K_P}{2} * \frac{W}{L}(V_{DD} - V_{THN})^2} \tag{11}$$

Then, the rising delay time is

$$t_{PLH} = R_{p2} * C_{tot} \tag{12}$$

and the corresponding falling delay time is

$$t_{PHL} = R_{n2} * C_{tot} \tag{13}$$

In each stage it has average current as

$$I_{avg} = \frac{QC_{tot}}{T} = \frac{V_{DD} * C_{tot}}{T} \tag{14}$$

and the overspending average power consumption of each stage is

$$P_{avg} = V_{DD} * I_{avg} = \frac{{V_{DD}}^2 * C_{tot}}{T} = C_{tot} * {V_{DD}}^2 * f_{osc} \tag{15}$$

The clock used needs to be non-overlapping. A clock generating circuit is illustrated in Figure 7.

However we propose a clock generator circuit as shown in Figure 8. The circuit is implemented by using five stages ring oscillator circuit. The oscillating frequency is controlled by the voltage Vref1 which is the output from bandgap circuit. As stated above and we restate here that the output voltage from the bandgap circuit is independent not only of the supply voltage but also with the temperature. Consequently the oscillator output frequency has small variation.

2.3 Operational Amplifier

Figure 9 is a one stage operational amplifier [7]. The characteristics of big signal of one stage operational amplifier will be discussed in sequel. When voltage V_{G1} is smaller than V_{G2}, M_1, M_3 and M_4 are off. The current of V_{DD} is zero. Meanwhile the M_2 and the M_5 are at deep triode region and they have zero output current. Therefore, the output voltage (V_{out}) is zero. When V_{G1} approaches V_{G2}, M_1 turns on and M_3 gets some current

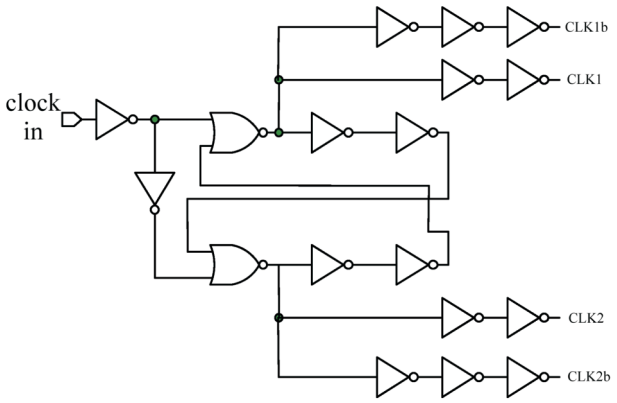

Figure 7. A non-overlap clock generator circuit.

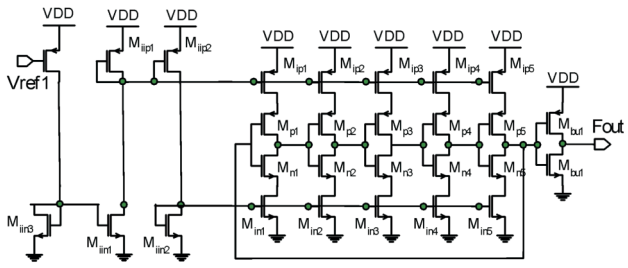

Figure 8. A five stage ring oscillator circuit.

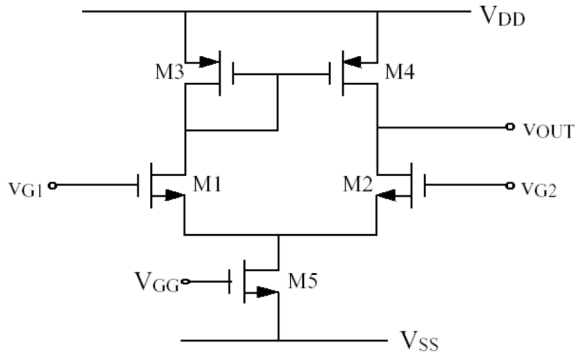

Figure 9. An one stage operation amplifier.

from the current of M_5 (I_{D5}) at the time when M_4 is turned on, the output voltage depends on the value of I_{D4} and I_{D2}. When V_{G1} is approximately equal to V_{G2}, M_2 and M_4 are in saturated region and their gains are increased. When VG1 is greater than V_{G2}, then the current of I_{D1}, I_{D3}, I_{D4} are increasing, while I_{D2} is decreasing. Eventually, M_4 will be in deep triode region. If V_{G1}-V_{G2} is large enough, M_2 will be turned off and M_4 is in deep triode region. AT this situation the current through the circuit is zero and the output voltage is kept the same as V_{DD}. The function of the op amp is the same as that of a comparator.

In the design of an operational amplifier, we use the following relationships to estimate the MOS size [7].

The open loop gain is

$$A_V = g_{m1}\,(r_{o2} \,||\, r_{o4}) = g_{m1}R_{out} \tag{16}$$

The -3dB bandwidth of the frequency response is

$$\varpi_{-3dB} = \frac{1}{R_{out}C_L} \tag{17}$$

The maximum and minimum common mode input voltages are:

$$V_{IC(\max)} = V_{DD} - V_{SG\,3}\_V_{TN\,1} \tag{18}$$

$$V_{IC\,(\min)} = V_{SS\,(sat)} - V_{GS\,1} = V_{DS\,5\,(sat)} + V_{GS\,2} \tag{19}$$

The slew rate is,

$$SR = I_5 / C_L \tag{20}$$

The power consumption can be calculated from:

$$P_{diss} = (V_{DD} + |V_{SS}|)(I_5) = (V_{DD} + |V_{SS}|)(I_3 + I_4) \tag{21}$$

2.4 Charge-Pump Circuit

We use charge pump-circuit to generate an output voltage that is greater than the supply voltage. A sample charge-pump circuit implemented with a capacitor and three switches is shown in Figure 10 [8]. When the clock is in phase 1, the switches S_1 and S_3 are closed, and the voltage of the capacitor is charged to V_{DD}. Then, when the clock is at pahse 2, the switches S_1 and S_3 are open, and the switch S_2 is closed. The output voltage is the sum of the supply voltage (V_{DD}) and the capacitor voltage. These results can be illustrated in the following equation [8].

$$(V_{out} - V_{DD}) * C = V_{DD} * C \tag{22}$$

or

$$V_{out} = 2 * V_{DD} \tag{23}$$

For this reason, the output voltage of the sample charge-pump circuit is double of the supply voltage at null loading.

By taking the loading effect into consideration, the circuit is modified as shown in Figure 11. The ideal output voltage is then change

$$V_{out} = \frac{C}{C + C_{out}} * 2 * V_{DD} \tag{24}$$

If the loading resistor (R_L) varies to a large extent, then the voltage across the loading resistor will also demonstrate large ripple voltage.

A complete charge pump circuit has the structure as known in Figure 12. The devices included in the red dotted line are the circuit external devices of the circuit.

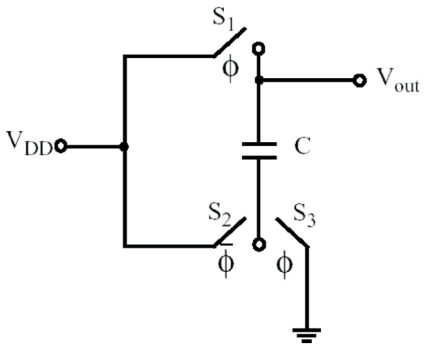

Figure 10. A sample charge pumping circuit.

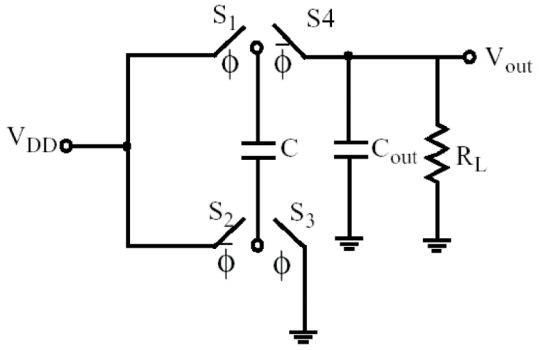

Figure 11. A practical charge pumping circuit.

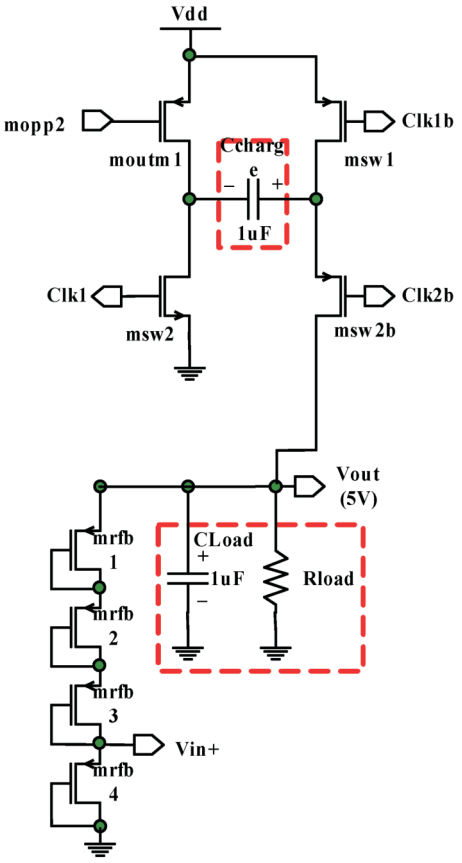

Figure 12. Charge pumping circuit.

When the clock is in the positive period, msw 1 and msw 2 are turned on, and moutm1 and msw 2b are turned off. It charges the capacitor, Ccharge, to the voltage as the same level as the supply voltage, V_{DD}. When clock is in negative period, then msw 1 and msw 2 are turned off, and moutm 1 and msw 2b are turned on. It charges the capacitor, C_{Load}, to the level of double the supply voltage, 2 V_{DD}. In order to get constant output voltage at 5 V, we use operational amplifier to control the voltage changing when the clock is in the negative period. The output voltage is divided among resistives of mrfb 1 to mrfb 4 and the divided voltage is feedback to the operational amplifier. The operational amplifier compares the reference voltage with the feedback voltage to control the switch, moutm 1, to turn it on or off. So we can control the output voltage not to reach the level of twice of the supply voltage but keeping at constant level.

2.5 White LED Driver Circuit

Figure 13 is the proposed functional block diagram of a parallel constructed White LED driver and its associated application circuit [9]. It has constant supply voltage to the White LED Driver, this supply voltage is greater than the forward bias of the White LED. It only needs three capacitors to boost the voltage in the application circuit, and it occupies only a small space. Because it does not use inductors, it does not introduce any Electromagnetic Interference (EMI). Since it does not induce any EMI and it only occupies a small space area, it is suitable for use in cell phones. However it has drawback that it supplies different amount of current to each White LED. Consequently it has different light efficiency and brightness for each While LED. However these variations in each White LED do not impose any noticeable response to the human eyes.

Figure 14(a) is an equivalent circuit of the circuit in Figure 13 [8]. When switches Sw 1 and Sw 3 are closed, Sw 2 and Sw 4 are open. The capacitor (C_{FLY}) is charged up to the supply voltage and the current flows in the loop is illustrated in Figure 14(b). When switches Sw 1 and Sw 3 are open, then switches Sw 2 and Sw 4 are closed. The capacitor (C_{out}) is charged up to the level of twice of the supply voltage. By using the feedback in the loop, the output voltage is maintained at constant level to avoid the redundant power consumption of the supply voltage.

3. Circuit Layout

The mask of the circuit layout is provided by mask provider, and the mask is then used by the foundry to fab-

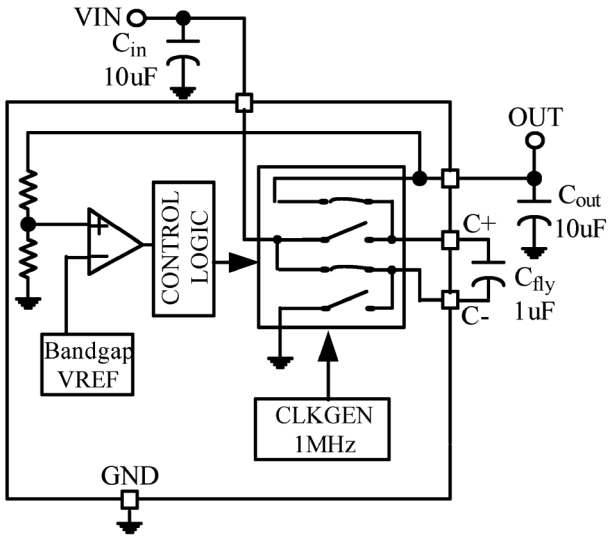

Figure 13. Functional block of White LED driver and its application circuit.

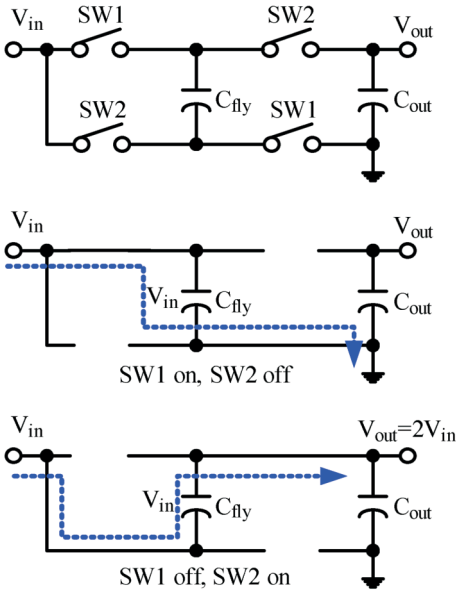

Figure 14. Equivalent circuit of White LED driver.

ricate IC. The following issues need be watched when layout the circuit. First, it needs to consider the matching of MOS transistors. For example, it needs to match the MOS transistors in the operational amplifier circuit. If the MOS transistors are not matching, it will have the result of generating large input offset voltage. Second, it needs to consider carefully the current density in the wires. If the wire width is too small, it may result in larger current so as to burn the wire. Third, it needs to isolate the analog circuit from the digital circuit to reduce the interference of the digital circuit on the analog circuit so as to decrease the characteristic variations of the analog circuits. Summarily, it needs to consider the configuration of the circuit layout, the wire width etc. The photographic layout of our IC is shown in Figure 15. The Die size is 1.45 mm × 1.45 mm with pads.

4. Measurement Results

Initially the supply voltage is set at 5.5 V, we then take measurements of the White LED output collage by decreasing in step of 0.1 V of the input voltage until the supply voltage reaches 2.5 V. The measured result is plotted in Figure 16. Table 1 summarizes the performance.

5. Conclusions

In this paper we used the architecture of charge-pump to design a White LED driver. In the design we used operational amplifier to control charge-pump circuit so as to maintain a constant driver output voltage. Consequently it avoids the unnecessary power consumption of the circuit.

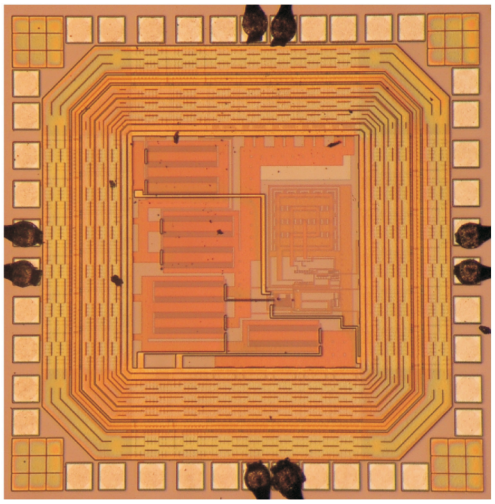

Figure 15. Layout of White LED driver.

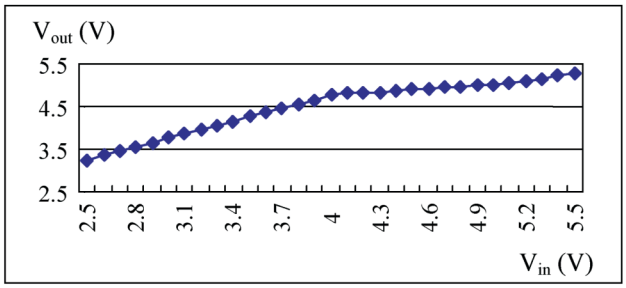

Figure 16. Measured output voltage of White LED driver.

Table 1. Performance summary

Technology	TSMC 0.35um 2P4M CMOS	
Area	1.45 mm × 1.45 mm	
	SPEC.	Measure
Supply Voltage	3.2V~5.5V	3.2V~5.5V
Output Voltage	4.7V~5.2V	4V~5.3V
Output Voltage Ripple	< 70 mV	< 100 mV
Output Current	100 mA	100 mA

References

[1] http://www.mas-oy.com/archive/da9251.pdf
[2] http://www.linear.com/pc/downloadDocument

.do?navId=H0,C1,C1003,C1042,C1031,C1061,P2114,D2139

[3] Allen, Phillip E. and Holberg, Douglas R., *CMOS Analog Circuit Design,* New York: Oxford University Press, 2002, Chapter 4, Analog CMOS Subcircuits.

[4] Behzad Razavi, *Design of Analog CMOS Integrated Circuit,* McGraw-Hill Companies, Inc, 2001, Chapter 11 Bandgap References.

[5] Jones, David A., Ken Martin, "Analog Integrated Circuit Design," John Wiley & Sons, Inc. 1997. Chapter 16, Phase-Locked Loops.

[6] Jacob Baker, R., Li, Harry W. and Boyce, David E., *CMOS Circuit Design, Layout, and Simulation,* New York: IEEE Press, 1998. Chapter 11, The Inverter.

[7] Allen, Phillip E. and Holberg, Douglas R., *CMOS Analog Circuit Design,* New York: Oxford University Press, 2002, Chapter 5, CMOS Amplifiers.

[8] Pylarinos, L., *Charge Pumps: An Overview,* University of Toronto, Tutorial Papers on Analog Circuits, 2002.

[9] http://www.eedesign.com.tw/html2/PaperD.asp?cid=4&xmlid=40118&channelid=10

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